

## REMARKS

Applicants respectfully request the Examiner's consideration of the present application as amended. Claims 1 and 14-32 remain in the application. No claims have been amended, canceled, or added.

Applicants respectfully submit that the claims are not anticipated by or rendered obvious over U.S. Pat. No. 6,467,009 of Winegarden ("Winegarden").

Winegarden discloses a configurable system on a chip, including configurable system logic, and a multimaster bus. However, with respect to configuration, Winegarden notes: /

The configuration process becomes infinitely flexible in which the on-chip CPU simply writes the configuration data to the appropriate configuration memory locations.

(Winegarden Col. 29, lines 48-51).

Claim 1 on the other hand, recites:

A method of using a multi-master system bus on a configurable system on a chip (CSoC), the CSoC including configurable system logic (CSL), the method comprising:  
controlling the multi-master system bus for configuration using a first device, the first device comprising a selectable one of an on-chip central processing unit (CPU), a direct memory access (DMA) controller, and an external control device;  
configuring a memory cell in the CSL using the multi-master system bus; and  
reading the memory cell in the CSL using the multi-master system bus.

(Claim 1). As noted above, Winegarden does not teach or suggest a multi-master system bus, which may be controlled by one of multiple masters *for configuration*. Therefore, claim 1, as amended, is not anticipated by Winegarden. Claims 2-3 and 14-20 depend on claim 1, and incorporate its limitations. Therefore, for

at least the same reasons advanced above with respect to claim 1, claims 14-20 are not anticipated by Winegarden.

Claim 21 recites:

A method of configuring a configurable system on a chip (CsoC) comprising:  
initiating configuration of the CsoC using an on-chip central processing unit (CPU);  
passing control of a multi-master system bus to a first device for configuring on-chip configurable system logic (CSL);  
configuring a memory cell in the CSL using the first device.

(Claim 21). As noted above, Winegarden does not teach or suggest "passing control of a multi-master system bus to a first device" from the CPU, for configuration. Rather, Winegarden specifically states that the CSL is configured using the on-board CPU. Therefore, claim 21, and claims 22-29 which depend on it, are not anticipated by or obvious over Winegarden.

Claim 30 recites:

A method comprising:  
initiating configuration of a configurable system on chip (CsoC) using an on-chip central processing unit (CPU);  
configuring a memory cell in the CSL using a first device of a group of devices, the group of devices comprising the CPU, a direct memory access (DMA) controller, and an external control device;  
reading a memory cell in the CSL using a second device selected from the group of devices; and  
selecting a signal in the CSoC to determine if the system bus is used for configuration or general interconnect of the CSoC.

(Claim 30). As noted above, Winegarden does not teach or suggest configuring a memory cell by a selected one of a set of possible devices. Therefore, claim 30, and claims 31 and 32 which depend on it, are not anticipated by or obvious over Gittinger.

Applicants respectfully submit that in view of the amendments and discussion set forth herein, the applicable rejections have been overcome. Accordingly the present and amended claims should be found to be in condition for allowance.


If the Examiner finds any remaining impediment to the prompt allowance of these claims that could be clarified with a telephone conference, the Examiner is respectfully requested to contact Judith A. Szepesi at (408) 720-8300.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due and not covered by any check submitted.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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